CLAIMS

1. (Original) A data processing device comprising:

a microprocessor for fetching and executing an instruction;

a coprocessor for storing data managed by the microprocessor;

a microprocessor data cache for storing data managed by the microprocessor;

an X-data cache for storing a first data group managed by the coprocessor; and

a Y-data cache for storing a second data group managed by the coprocessor.

2. (Original) The data processing device of claim 1, wherein the microprocessor conducts arithmetic operations for integers and floating points, and Boolean functions.

3. (Original) The data processing device of claim 1, wherein the coprocessor executes a digital signal processor function operable with at least one of video, audio, video capture and play-back, telephone communication, voice identification and synthesis, and multimedia communication.

4. (Original) The data processing device of claim 3, wherein the digital signal processor function is micro-coded with at least one of finite impulse response and infinite impulse response filters, a Fourier transform, a correlation function, a matrix multiplication, and a Taylor series function.

5. (Original) A data processing device comprising:

a microprocessor for fetching and executing an instruction;

a coprocessor for storing data managed by the microprocessor;

an X-data cache for storing a first data group managed by the coprocessor; and

a Y-data cache for storing a second data group managed by the coprocessor;

wherein the microprocessor selects an alternative one of the X-data cache and the Y-data cache to store data managed by the microprocessor.

6. (Original) The data processing device of claim 5, wherein the microprocessor conducts arithmetic operations for integers and floating points, and Boolean functions.

7. (Original) The data processing device of claim 5, wherein the coprocessor executes a digital signal processor function operable with at least one of video, audio, video capture and play-back, telephone communication, voice identification and synthesis, and multimedia communication.

8. (Original) The data processing device of claim 7, wherein the digital signal processor function is micro-coded with at least one of finite impulse response and infinite impulse response filters, a Fourier transform, a correlation function, a matrix multiplication, and a Taylor series function.

9. (Original) A computer system comprising:

a system bus;

a host processor for receiving, decoding, and executing an instruction;

an arbiter for controlling priorities for system bus access;

a data processing unit for performing a digital signal processing operation subject to the host processor; and

an external memory for storing data managed by the data processing unit;

wherein the data processing unit comprises:

a microprocessor for fetching and executing an instruction;

a coprocessor for storing data managed by the microprocessor;

a microprocessor data cache for storing data managed by the microprocessor;

an X-data cache for storing a first data group managed by the coprocessor; and

a Y-data cache for storing a second data group managed by the coprocessor.

10. (Original) The computer system of claim 9, further comprising a slave in accordance with a need of a user.

11. (Original) The computer system of claim 10, wherein the slave comprises at least one of a storage extension module, a video control extension module, a multimedia extension module, and a communication extension module.

12. (Original) The computer system of claim 10, further comprising a decoder for addressing the data processing unit and the slave.

13. (Original) The computer system of claim 9, wherein the external memory comprises: a microprocessor data field for storing data to and/or from the microprocessor data cache; an X-

data field for storing to and/or from the X-data cache, and a Y-data field for storing to and/or from the Y-data cache.

14. (Original) The data processing device of claim 9, wherein the microprocessor conducts arithmetic operations for integers and floating points, and Boolean functions.

15. (Original) The data processing device of claim 9, wherein the coprocessor executes a digital signal processor function operable with at least one of video, audio, video capture and play-back, telephone communication, voice identification and synthesis, and multimedia communication.

16. (Original) The data processing device of claim 15, wherein the digital signal processor function is micro-coded with at least one of finite impulse response and infinite impulse response filters, a Fourier transform, a correlation function, a matrix multiplication, and a Taylor series function.

17. (Original) A computer system comprising:

a system bus;

a host processor for receiving, decoding, and executing an instruction;

an arbiter for controlling priorities for system bus access;

a data processing unit for performing a digital signal processing operation subject to the host processor; and

an external memory for storing data managed by the data processing units;

wherein the data processing unit comprises:

a microprocessor for fetching and executing an instruction;

a coprocessor for storing data managed by the microprocessor;

an X-data cache for storing a first data group managed by the coprocessor; and

a Y-data cache for storing a second data group managed by the coprocessor.

18. (Original) The computer system of claim 17, further comprising a slave in accordance with a need of a user.

19. (Original) The computer system of claim 18, wherein the slave comprises at least one of a storage extension module, a video control extension module, a multimedia extension module, and a communication extension module.

20. (Original) The computer system of claim 18, further comprising a decoder for addressing the data processing unit and the slave.

21. (Previously Presented) The computer system of claim 17, wherein the external memory comprises:

a microprocessor data field for storing data to and/or from the microprocessor;

an X-data field for storing to and/or from the X-data cache; and

a Y-data field for storing to and/or from the Y-data cache, wherein the X-data field and the Y-data field overlap, and wherein an area of overlap is the microprocessor data field.

22. (Original) The data processing device of claim 17, wherein the microprocessor conducts arithmetic operations for integers and floating points, and Boolean functions.

23. (Original) The data processing device of claim 17, wherein the coprocessor executes a digital signal processor function operable with at least one of video, audio, video capture and play-back, telephone communication, voice identification and synthesis, and multimedia communication.

24. (Original) The data processing device of claim 23, wherein the digital signal processor function is micro-coded with at least one of finite impulse response and infinite impulse response filters, a Fourier transform, a correlation function, a matrix multiplication, and a Taylor series function.

25. (Previously Presented) The data processing system of claim 5, further comprising an external memory segmented into an X-data field for storing data of the X-data cache, a Y-data field for storing data of the Y-data cache, and a microprocessor data field, wherein the X-data field and the Y-data field overlap, and wherein an area of overlap is the microprocessor data field.